CLAIMS

What is claimed is:

1. A variable oscillator circuit on a semiconductor device, comprising:

a ring oscillator for producing a variable frequency-oscillating signal including:

a base delay stage; and

a variable delay stage having a delay selection signal that selects a programmable delay magnitude, wherein

the base delay stage and the variable delay stage connect in a ring having an odd number of logical inversions;

a frequency analyzer for converting the variable frequency-oscillating signal to an encoded actual frequency signal;

a frequency comparator wherein the encoded actual frequency signal is compared to an encoded desired frequency input to generate a frequency deviation result; and

a frequency modifier for generating the delay selection signal based on the frequency deviation result.

2. The circuit of claim 1, wherein the variable delay stage comprises:

a plurality of delay elements connected in series producing a series of sequentially delayed output taps; and

a delay selector for creating the programmable delay magnitude by selecting one of the series of sequentially delayed output taps based on the delay selection signal.

3. The circuit of claim 1, wherein the variable delay stage comprises:

a buffer element having a buffer element output signal;

a plurality of load elements connected in parallel to the buffer element output signal; and

a load selector for creating the programmable delay magnitude by enabling connection of a variable number of the plurality of load elements to the buffer element output signal based on the delay selection signal.

4. The circuit of claim 1, wherein the frequency modifier comprises:

an input divide clock operably coupled to the variable frequency-oscillating signal;

a clock divider for determining an update rate to the variable frequency-oscillating signal by dividing the input divide clock by a predetermined programmable rate;

a deviation sampler for generating a sampled frequency deviation result based on sampling the frequency deviation result at the update rate; and

a deviation encoder for generating the delay selection signal based on the sampled frequency deviation result.

5. The circuit of claim 1, wherein the frequency analyzer comprises:

an input sample clock operably coupled to the variable frequency-oscillating signal;

an input reference clock operably coupled to the variable frequency-oscillating signal;

a clock sampler comprising:

a plurality of clock delay elements operably coupled to the input sample clock and connected in series producing a series of sequentially delayed clocks; and

a plurality of sample elements each of the plurality of sample elements using one of the series of sequentially delayed clocks to sample the input reference clock and producing a plurality of sequentially delayed clock samples; and

an actual frequency encoder comprising:

a transition counter for producing a delay count indicating the number of the plurality of sequentially delayed clock samples between two consecutive active edges; and

an encoder for converting the delay count to the encoded actual frequency signal.

6. A variable oscillator circuit on a semiconductor device, comprising:
a sample clock oscillator having a sample clock frequency;
a ring oscillator for producing a variable frequency-oscillating signal including:
a base delay stage; and
a variable delay stage having a delay selection signal that selects a programmable delay magnitude, wherein
the base delay stage and the variable delay stage connect in a ring having an odd number of logical inversions;
a frequency analyzer operating at the sample clock frequency for converting the variable frequency-oscillating signal to an encoded actual frequency signal;
a frequency comparator wherein the encoded actual frequency signal is compared to an encoded desired frequency input to generate a frequency deviation result; and
a frequency modifier for generating the delay selection signal based on the frequency deviation result.

7. The circuit of claim 6, further comprising an encoded calibration input wherein the encoded calibration input produces variations in the frequency of the sample clock oscillator.

8. The circuit of claim 6, wherein the variable delay stage comprises:
a plurality of delay elements connected in series producing a series of sequentially delayed output taps; and
a delay selector for creating the programmable delay magnitude by selecting one of the series of sequentially delayed output taps based on the delay selection signal.

9. The circuit of claim 6, wherein the variable delay stage comprises:
a buffer element having a buffer element output signal;
a plurality of load elements connected in parallel to the buffer element output signal; and
a load selector for creating the programmable delay magnitude by enabling connection of a variable number of the plurality of load elements to the buffer element output signal based on the delay selection signal.

10. The circuit of claim 6, wherein the frequency modifier comprises:

an input divide clock operably coupled to the variable frequency-oscillating signal;

a clock divider for determining an update rate to the variable frequency-oscillating signal by dividing the input divide clock by a predetermined programmable rate;

a deviation sampler for generating a sampled frequency deviation result based on sampling the frequency deviation result at the update rate; and

a deviation encoder for generating the delay selection signal based on the sampled frequency deviation result.

11. The circuit of claim 6, wherein the frequency analyzer comprises:

an input sample clock operably coupled to the sample clock frequency;

an input reference clock operably coupled to the variable frequency-oscillating signal;

a clock sampler comprising:

a plurality of clock delay elements operably coupled to the input sample clock and connected in series producing a series of sequentially delayed clocks; and

a plurality of sample elements each of the plurality of sample elements using one of the series of sequentially delayed clocks to sample the input reference clock and producing a plurality of sequentially delayed clock samples; and

an actual frequency encoder comprising:

a transition counter for producing a delay count indicating the number of the plurality of sequentially delayed clock samples between two consecutive active edges; and

an encoder for converting the delay count to the encoded actual frequency signal.

12. The circuit of claim 6, wherein the frequency analyzer comprises:
an input sample clock operably coupled to the sample clock frequency;
an input reference clock operably coupled to the variable frequency-oscillating signal;
a clock sampler comprising, a plurality of sample elements connected in series using the input reference clock to sample the input reference clock and producing a plurality of sequentially delayed clock samples; and
an actual frequency encoder comprising:
a transition counter for producing a delay count indicating the number of the plurality of sequentially delayed clock samples between two consecutive active edges; and
an encoder for converting the delay count to the encoded actual frequency signal.

13. A variable oscillator circuit on a semiconductor device, comprising:
a reference input clock;
a ring oscillator producing a variable frequency-oscillating signal including:
a base delay stage; and
a variable delay stage having a delay selection signal that selects a programmable delay magnitude, wherein
the base delay stage and the variable delay stage connect in a ring having an odd number of logical inversions;
a first frequency analyzer for converting the variable frequency-oscillating signal to an encoded actual frequency signal;
a second frequency analyzer for converting the reference input clock to an encoded desired frequency signal;
a frequency comparator wherein the encoded actual frequency signal is compared to the encoded desired frequency signal to generate a frequency deviation result; and
a frequency modifier for generating the delay selection signal based on the frequency deviation result.

14. The circuit of claim 13, further comprising a phase adjuster for producing a phase adjusted variable frequency-oscillating signal by modifying the phase delay of the variable frequency-oscillating signal to match the phase of the reference input clock.

15. The circuit of claim 13, wherein the variable delay stage comprises:
a plurality of delay elements connected in series producing a series of sequentially delayed output taps; and
a delay selector for creating the programmable delay magnitude by selecting one of the series of sequentially delayed output taps based on the delay selection signal.

16. The circuit of claim 13, wherein the variable delay stage comprises:
a buffer element having a buffer element output signal;
a plurality of load elements connected in parallel to the buffer element output signal; and
a load selector for creating the programmable delay magnitude by enabling connection of a variable number of the plurality of load elements to the buffer element output signal based on the delay selection signal.

17. The circuit of claim 13, wherein the frequency modifier comprises:
an input divide clock operably coupled to the variable frequency-oscillating signal;
a clock divider for determining an update rate to the variable frequency-oscillating signal by dividing the input divide clock by a predetermined programmable rate;
a deviation sampler for generating a sampled frequency deviation result based on sampling the frequency deviation result at the update rate; and
a deviation encoder for generating the delay selection signal based on the sampled frequency deviation result.

18. The circuit of claim 13, wherein the first frequency analyzer comprises:
an input sample clock operably coupled to the variable frequency-oscillating signal;
an input reference clock operably coupled to the variable frequency-oscillating signal;
a clock sampler comprising:

a plurality of clock delay elements operably coupled to the input sample clock and connected in series producing a series of sequentially delayed clocks; and

a plurality of sample elements each of the plurality of sample elements using one of the series of sequentially delayed clocks to sample the input reference clock and producing a plurality of sequentially delayed clock samples; and

an actual frequency encoder comprising:

a transition counter for producing a delay count indicating the number of the plurality of sequentially delayed clock samples between two consecutive active edges; and

an encoder for converting the delay count to the encoded actual frequency signal.

19. The circuit of claim 13, wherein the second frequency analyzer comprises:

a second input sample clock operably coupled to the reference input clock;

a second input reference clock operably coupled to the reference input clock;

a second clock sampler comprising:

a second plurality of clock delay elements operably coupled to the second input sample clock and connected in series producing a second series of sequentially delayed clocks; and

a second plurality of sample elements each of the second plurality of sample elements using one of the second series of sequentially delayed clocks to sample the second input reference clock and producing a second plurality of sequentially delayed clock samples; and

a second actual frequency encoder comprising:

a second transition counter for producing a second delay count indicating the number of the second plurality of sequentially delayed clock samples between two consecutive active edges; and

a second encoder for converting the second delay count to the encoded desired frequency signal.

20. A system of synchronized semiconductor devices comprising:

a first semiconductor device comprising:

a ring oscillator producing a variable frequency-oscillating signal including:

a base delay stage; and

a variable delay stage having a delay selection signal that selects a programmable delay magnitude, wherein

the base delay stage and the variable delay stage connect in a ring having an odd number of logical inversions;

a frequency analyzer for converting the variable frequency-oscillating signal to an encoded actual frequency signal;

a frequency comparator wherein the encoded actual frequency signal is compared to an encoded desired frequency input to generate a frequency deviation result; and

a frequency modifier for generating the delay selection signal based on the frequency deviation result; and

at least one additional semiconductor device comprising:

a reference input clock connected to the variable frequency-oscillating signal of the first semiconductor device;

an additional ring oscillator producing an additional variable frequency-oscillating signal including:

an additional base delay stage; and

an additional variable delay stage having an additional delay selection signal that selects an additional programmable delay magnitude, wherein

the additional base delay stage and the additional variable delay stage connect in a ring having an odd number of logical inversions;

a first frequency analyzer for converting the additional variable frequency-oscillating signal to an additional encoded actual frequency signal;

a second frequency analyzer for converting the reference input clock to an encoded desired frequency signal;

a frequency comparator wherein the additional encoded actual frequency signal is compared to the encoded desired frequency signal to generate an additional frequency deviation result; and

an additional frequency modifier for generating the additional delay selection signal based on the additional frequency deviation result.

21. A method for modifying a frequency of an oscillating signal comprising:

generating a variable frequency-oscillating signal using a ring oscillator having a programmable delay magnitude;

analyzing the variable frequency-oscillating signal to develop an encoded actual frequency signal;

comparing the encoded actual frequency signal to an encoded desired frequency input to generate a frequency deviation result; and

modifying the programmable delay magnitude and thereby the variable frequency-oscillating signal based on the frequency deviation result.

22. A method for modifying a frequency of an oscillating signal comprising:
generating a sample clock frequency using a sample clock oscillator;
generating a variable frequency-oscillating signal using a ring oscillator having a programmable delay magnitude;
analyzing the variable frequency-oscillating signal using the sample clock frequency to develop an encoded actual frequency signal;
comparing the encoded actual frequency signal to an encoded desired frequency input to generate a frequency deviation result; and
modifying the programmable delay magnitude and thereby the variable frequency-oscillating signal based on the frequency deviation result.

23. A method for modifying a frequency of an oscillating signal comprising:
generating a variable frequency-oscillating signal using a ring oscillator having a programmable delay magnitude;
analyzing the variable frequency-oscillating signal to develop an encoded actual frequency signal;
analyzing a reference input clock to develop an encoded desired frequency signal;
comparing the encoded actual frequency signal to the encoded desired frequency signal to generate a frequency deviation result; and
modifying the programmable delay magnitude and thereby the variable frequency-oscillating signal based on the frequency deviation result.

24. A variable oscillator circuit on a semiconductor device, comprising:
a means for producing a variable frequency-oscillating wherein the frequency is varied based on a delay selection signal;
a means for analyzing the frequency of the variable frequency-oscillating signal and converting the analysis results to an encoded actual frequency signal;
a means for comparing the encoded actual frequency signal to an encoded desired frequency input and generating a frequency deviation result; and
a means for generating the delay selection signal based on the frequency deviation result.

25. A variable oscillator circuit on a semiconductor device, comprising:

a means for generating a sample clock frequency;

a means for producing a variable frequency-oscillating wherein the frequency is varied based on a delay selection signal;

a means for analyzing the frequency of the variable frequency-oscillating signal operating at the sample clock frequency and converting the analysis results to an encoded actual frequency signal;

a means for comparing the encoded actual frequency signal to an encoded desired frequency input and generating a frequency deviation result; and

a means for generating the delay selection signal based on the frequency deviation result.

26. A variable oscillator circuit on a semiconductor device, comprising:

a means for producing a variable frequency-oscillating wherein the frequency is varied based on a delay selection signal;

a means for analyzing the frequency of the variable frequency-oscillating signal and converting the analysis results to an encoded actual frequency signal;

a means for analyzing the frequency of a reference input clock and converting the analysis results to an encoded desired frequency signal;

a means for comparing the encoded actual frequency signal to the encoded desired frequency input and generating a frequency deviation result; and

a means for generating the delay selection signal based on the frequency deviation result.